

Call for Papers

Special Issue of IEEE Transactions on Nanotechnology: *Revolutionary 3-D Integration and Design for Next Generation Computing*

Background and Scope

As the scaling limitations of 2-D ICs are becoming more apparent, 3-D integration at nanoscale is emerging as an attractive alternative to continue IC scaling in the future. Driven by the benefits of less stringent lithographic dependence, multi-scale nature with reduced interconnections, higher packing density and smaller footprints, 3-D ICs promise to revolutionize the semiconductor and computing industries and enable unique new applications. Promising 3-D IC directions include nanoscale monolithic and fine-grained 3-D CMOS and beyond CMOS 3-D approaches, as well as heterogeneous technologies that are multi-scale in nature, with potentially orders of magnitude improved efficiencies. 3-D IC research often involves cross-disciplinary explorations at multiple scales, combining new technologies for manufacturing and devices with unique integration/design concepts. Targeting the broad device, circuit, and architecture, as well as nanotechnology research communities, this special issue seeks papers on innovative new concepts for such 3-D ICs. High-risk high-reward type of ideas, rethinking 3-D integration, and associated circuits and architectures, will be preferred to incremental research. Applications that are enabled by or show potential for significant benefits from 3-D integration are also welcome. Review papers presenting a broad overview of emerging 3-D technologies can be similarly submitted.

Topics of interest include but are not limited to the following:

- 3-D IC integration and 3-D fabrics enabled by emerging nanotechnology.
- 3-D memory and logic technologies.
- 3-D routability.
- 3-D circuit design exploration with CMOS and beyond CMOS directions.
- 3-D circuit architectural exploration with CMOS and beyond CMOS directions.
- Unconventional computing paradigms such as neuromorphic, probabilistic, sparse data and others, enabled by 3-D integration.
- Gate and transistor-level monolithic 3-D CMOS directions.
- Multi-scale, mixed-signal heterogeneous 3-D integrations.
- 3-D design methodologies including thermal management.
- New applications enabled by or significantly benefitting from 3-D integration.
- Experimental proof-of-concept prototyping for small-scale demonstrations as well as scalable 3-D nanomanufacturing approaches. Directions may include multi-level epitaxial growth, wafer thinning, wafer bonding, and wafer alignment techniques, as well as others.

Submission Format

The submitted papers must be written in English and describe original research which is not published nor currently under review by other journals or conferences. Extended conference papers should contain at least 50% new material and will pass through the normal review process. Author guidelines for preparation of manuscript can be found at the IEEE Transactions on Nanotechnology website (<http://sites.ieee.org/tnano/author-info/>).

Submission Guidelines

All manuscripts and any supplementary material should be submitted through the TNANO Manuscript Central (<http://mc.manuscriptcentral.com/tnano>). On submission, authors must select the “*Special Issue*” manuscript type instead of “*Regular Paper*”, and state in the cover letter that the paper is for the special issue on “*Revolutionary 3-D Integration and Design for Next Generation Computing*,” and select Csaba Moritz as the *Preferred Editor*.

Important Dates

- Paper Submission: August 1, 2016 through December 1, 2016
- Reviews Completed: March 1, 2017
- Major Revisions Due (if Needed): April 1, 2017
- Minor Revisions Due (if Needed): June 1, 2017
- Notification of Final Acceptance: August 1, 2017
- Final Manuscript Due: Sept 1, 2017
- Tentative Publication Date: Late 2017

Guest Editors

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